REMARKS

In the Office Action mailed December 26, 2002:

Claims 1-37 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-7, 19 and 29-36, to the extent understood, were rejected under 35 U.S.C. 102(b) as being anticipated by the Hoeld reference (U.S. Patent 5,639,680).

Claim 20 was indicated to be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph. Presumably, claims 21-28 which are dependent on claim 20 are also allowable.

Claims 8-18 and 37 were indicated to be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, and to include all of the limitations of the base claim and any intervening claims.

Claims 1, 20, and 29 have been amended to refer to " a reference voltage" as "a reference voltage signal", thereby providing a clear antecedent for the term refernce voltage signal used elsewhere in these claims. Dependent Claims 36 and 37 have also been amended to refer to the reference voltage signal. These changes are not believed to change the scope of these claims. Claims 2, 21 and 33 have been amended to refer to "input/output standard" as the "input/ output supply signal standard." Since each of these claims already refers to this standard as having a specified input/ output supply signal level, it is also believed that these changes do not change the scope of these claims.

Reconsideration of these rejections is respectfully requested.

THE REJECTIONS UNDER 35. U.S.C. 112 SHOULD BE WITHDRAWN

The present invention relates to a circuit for use with a variety of different input/output standards that use different input signals. As set forth at page 2, lines 15-20 of the specification, a switch circuit is needed to pass a reference voltage to input/ output buffer circuits for those input/output standards that require use of a reference voltage and to block such reference voltage for those input/ output standards that do not require such use. Prior art switch circuits, however, are often incapable of adequately passing the reference voltage to the input/ output buffers because the input/ output power supply that powers the switch circuit for a voltage-referenced standard is too low.

Claim 1 recites a switch circuit for selectively providing a reference voltage to a logic device, e.g., PLD, comprising a transmission switch circuit that receives the reference voltage signal at an input thereof and passes the reference voltage signal to an output thereof in response to a first control signal. In accordance with the invention, the first control signal has a logic level determined by a dedicated power supply signal that is different from the input/output power supply signal for the logic device. As a result the level of the control

signal is not determined by the input/ output power supply signal; and the problems of prior art switch circuits can be avoided.

The Examiner contends that claim 1 is indefinite because its limitations "an input/output supply signal", on line 6, and "the reference voltage signal" at times 1 and 3 appear to represent the same signal since the reference voltage signal is seen at the output of the switching circuit.

Applicants respectfully disagree. As explained in the specification at page 2, lines 1-9, the reference voltage signal is a signal that is provided to one input of each differential amplifier in an IC device operating under a voltage-referenced input/ output standard. The present invention provides a switch as described in claim 1 for selectively passing such a reference voltage signal to a logic device. In contrast, as explained at page 1, lines 15-16, the input/ output power supply signal provides power to the IC device to drive input/ output signals over the system bus. Plainly, the input/output supply signal is a different signal from the reference voltage signal. Indeed, in some embodiments of the invention, the input/ output supply signal is used by the switch circuit to control the passage of the reference voltage signal through the switch circuit. For example, in the embodiment of Fig. 1, VREF is "the reference voltage signal" and VCC-IO is "an input/ output supply signal". For these reasons, it is submitted that claim 1 is definite under 35 U.S.C. 112, second paragraph.

The Examiner contends that claim 2 is incomplete because the recitation of claim does not define "input/output standards", line 2, and claims 21 and 33 have the same problem. In addition, the Examiner asserts that the meaning of "voltage-referenced standard" at lines 3-4 and 5-6 of these claims is also unclear.

The limitation "each having a specified input/output supply signal level" in claim 2, line 2, provides the necessary definition for "input/output standards". The limitation "voltage-referenced standard" is indicated to be one of the plurality of input/output supply signal standards. The Background of the Invention indicates at page 1, lines 24-27 that there are a variety of input/ output standards having different VCC-IO requirements and either single-ended, differential or voltage-referenced input signals. Several examples of these standards are enumerated at page 1, line 27 to page 2, line 9. In view of this discussion, it is submitted that the meaning of "input/ output standards" and "voltage-referenced standard" will be abundantly clear to one of ordinary skill in the art and that claims 2, 21, and 33 are complete and definite under 35 U.S.C. 112, second paragraph.

The Examiner contends that the limitation "the input/output supply signal" in claims 9 and 15 lacks antecedent basis.

The limitation "an input/output supply signal" in claim 1 is clearly the antecedent for the limitation "the input/output supply signal" in claim 9. Therefore, claim 9 is definite under 35 U.S.C. 112, second paragraph.

The limitation "the input/ output supply signal" does not appear in claim 15, but does appear in claim 16. Again, the antecedent for this term is found in claim 1.

The Examiner contends that claims 11 and 20 are misdescriptive because Figure 1 shows the master control signal (VREF_CONTROL) being unrelated to the logic device (140). In addition, the limitation "the first supply signal is a core supply signal" is deemed to make no sense because "the first supply signal" and "the master control signal" refer to the same entity as recited on lines 2-3 of claim 8.

Number 140 in Figure 1 does not refer to a logic device. Instead, number 140 refers to an input buffer which is only one element of a logic device. *See* page 6, lines 31-32. The master control signal (VREF_CONTROL) is an input to logic level shift circuit 120 from a logic device core (not shown in Figure 1). *See* page 5, lines 25-26.

In addition, "the first supply signal" and "the master control signal" do not necessarily refer to the same entity, because claim 8 recites "the master control signal having a logic level determined by a first supply signal". This language clearly demonstrates that these two signals are related to each other through the master control signal's logic level, but not necessarily the same. Therefore, claims 11 and 20 are definite under 35 U.S.C. 112, second paragraph.

Claims 3-8, 10, 12-14, 16-19, 22-28, 30-32 and 34-37 are dependent from the rejected claims discussed above. Therefore, they are definite under 35 U.S.C. 112, second paragraph for at least the same reasons their independent claims are definite under 35 U.S.C. 112, second paragraph.

With the above arguments, the Applicants have addressed the 35 U.S.C. 112, second paragraph, rejections in the Office Action mailed December 26, 2002. Therefore, the rejections should be withdrawn.

THE REJECTIONS UNDER 35. U.S.C. 102 SHOULD BE WITHDRAWN

The Examiner has rejected claims 1-7, 19 and 29-36, to the extent understood, under 35 U.S.C. 102(b) as anticipated by the Hoeld reference (U.S. Patent 5,639,680).

Hoeld teaches an input cell circuit for use in a mixed signal mode where an input pin may receive either digital or analog signals. The circuit prevents leakage current between the input of the cell and the output of the cell.

It is the Examiner's position that Hoeld discloses in Fig. 4 a transmission switch circuit for passing a reference voltage signal that operates in response to a first control signal having a logic level determined by a dedicated supply signal VCC that is different from the reference voltage signal.

This, however, is not what is claimed in claim 1 where the control signal is required to have a logic level determined by a dedicated supply signal that is different from an input/ output supply signal. As emphasized above, the input/ output supply signal of applicants'

claim is not the reference voltage signal. Accordingly, since Hoeld does not teach each of the elements recited in claim 1, claim 1 is not anticipated by the Hoeld reference.

With respect to claim 2, the Examiner notes that Hoeld discloses a circuit for solving problems when the reference voltage is higher than Vcc+Vbe and argues that Hoeld's circuit is therefore inherently suitable for the dedicated voltage VCC having a level higher that that of the reference voltage signal. Again, however, the Exmainer has misunderstood the claim.

Claim 2 recites a switch circuit wherein the dedicated supply signal has a voltage level greater than the lowest specified input/output supply signal level for any voltage-referenced standard. In the embodiment of Figure 1, VCC_IO is the the lowest specified input/output supply signal, VCC_DED is the dedicated supply signal, and VREF is the reference voltage signal. In brief, claim 2 requires that the dedicated supply signal such as VCC_DED have a voltage level greater than the lowest specified input/ output supply signal level such as VCC_IO, not VREF. Further disclosure can be found on page 9, lines 31-32 of the specification.

For these reasons, it is respectfully submitted that Hoeld does not teach that the dedicated supply signal have a voltage level higher than the lowest specified input/output supply signal level for any voltage-referenced standard. Therefore, claim 2 is not anticipated by the Hoeld reference.

Claims 3-7 and 19 ultimately depend from claim 1. Therefore, claims 3-7 and 19 are not anticipated by the Hoeld reference for at least the same reason that claim 1 is not anticipated by the Hoeld reference.

Claims 29-36 recite method/steps related to the apparatus recited in claims 1-7. Therefore, claims 29-36 are not anticipated by the Hoeld reference for at least the same reason that claims 1-7 are not anticipated by the Hoeld reference.

While claims 8-18, 20 and 37 have been indicated to be allowable if rewritten to avoid 35 U.S.C. 112 rejections, the Examiner has not explicitly indicated the status of claims 21-28 with respect to prior art. It is respectfully submitted that these changes are patentable because these claims are dependent on claim 20 which has been indicated to be patentable.

In view of the foregoing, applicants believe that all of the claims are now in condition for allowance and respectfully requests the Examiner to pass the subject application to issue. If for any reason the Examiner believes any of the claims are not in condition for allowance, he is encouraged to phone the undersigned at (650) 849-7777 so that any remaining issues may be resolved.

Aside from the fee for an extension of time, no additional fee is believed due for filing this response. However, if a fee is due, please charge such fee to Pennie & Edmonds LLP's Deposit Account No. 16-1150.

Respectfully submitted,

Date: June 26, 2003

24,615
(Reg. No.)

Francis E. Morris
PENNIE & EDMONDS LLP
1155 Avenue of the Americas
New York, NY 10036-2811
(650) 849-7777

Listing of Claims

Claims 1 - 2	Currently amended.
Claims 3 - 19	Original.
Claims 20 - 21	Currently amended.
Claims 22 - 28	Original.
Claim 29	Currently amended.
Claims 30 - 32	Original.
Claim 33	Currently amended.
Claims 34 - 35	Original.
Claims 36 - 37	Currently amended.